

ECUcore-9263

Hardware Manual

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	WORLDWIDE
Address:	SYS TEC electronic GmbH August-Bebel-Str. 29 D-07973 Greiz GERMANY
Ordering Information:	+49 (3661) 6279-0 info@systec-electronic.com
Technical Support:	+49 (3661) 6279-0 support@systec-electronic.com
Fax:	+49 (3661) 62 79 99
Website:	http://www.systec-electronic.com

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1 Introduction

This manual describes the function and technical data for the ECUcore-9263, but not for the microcontroller Atmel AT91SAM9263 or any other supplemental products. Please refer to the corresponding manuals and documentation for any other products you may use.

Low-active signals are denoted by a „/“ in front of the signal name (i.e. “/RD”). The representation “0” indicates a logical-zero or low-level signal. A “1” is the synonym for a logical one or high-level signal.

2 Ordering Information and Support

Order Number	Version
4001017	ECUcore-9263
KIT-162	Development Kit ECUcore-9263

The ECUcore-9263 features:

- Atmel AT91SAM9263 MCU with 240 MHz
- Up to 128MiB NOR-FLASH
- Up to 256MiB NAND-FLASH
- Up to 64MiB SDRAM
- Up to 2MiB Video RAM (only 1MiB useable)
- Micro SD-Card slot
- Ethernet PHY
- CAN controller
- LVDS controller
- Touch controller
- Real time clock
- Reset/Watchdog IC
- Temperature sensor
- Single power supply 3,3V (all other voltages are derived onboard)
- ESD Handling Instructions (printed version)

The Development Kit includes the ECUcore module and a Development Board which allows for rapid application development.

The most important Development Board features:

- Touchscreen display
- Power supply connector 9-24VDC and an external power supply
- Dipswitch (8pos.), two rotary switches, some Keys and LEDs to test IO functionality
- Connectors for RS232, CAN, USB and Ethernet interfaces
- Audio input and output connectors
- SD card socket

- Boot and Reset button
- Battery for buffering RTC
- Matrix keypad (4x4)
- Expansion connector for developing user periphery

Software Support:

- Integrated Development Environment with complete GNU toolchain for ARM architecture
- uboot bootloader (pre-installed)
- Linux
 - plc-firmware (PLCcore-9263)
- CANopen protocol stack (limited function, obj-code library)
- CANopen Configuration Suite (Evaluation Version)
- CAN-Report CAN-bus monitor (Evaluation Version)
- OD-Builder

3 Properties of the ECUcore-9263

3.1 Overview

The ECUcore-9263 belongs to SYS TEC's ECUcore family. The ECUcore-9263 combines all elements of a microcontroller system on one board. With the help of modern SMD packages and the multilayer design, the module was designed at minimum size.

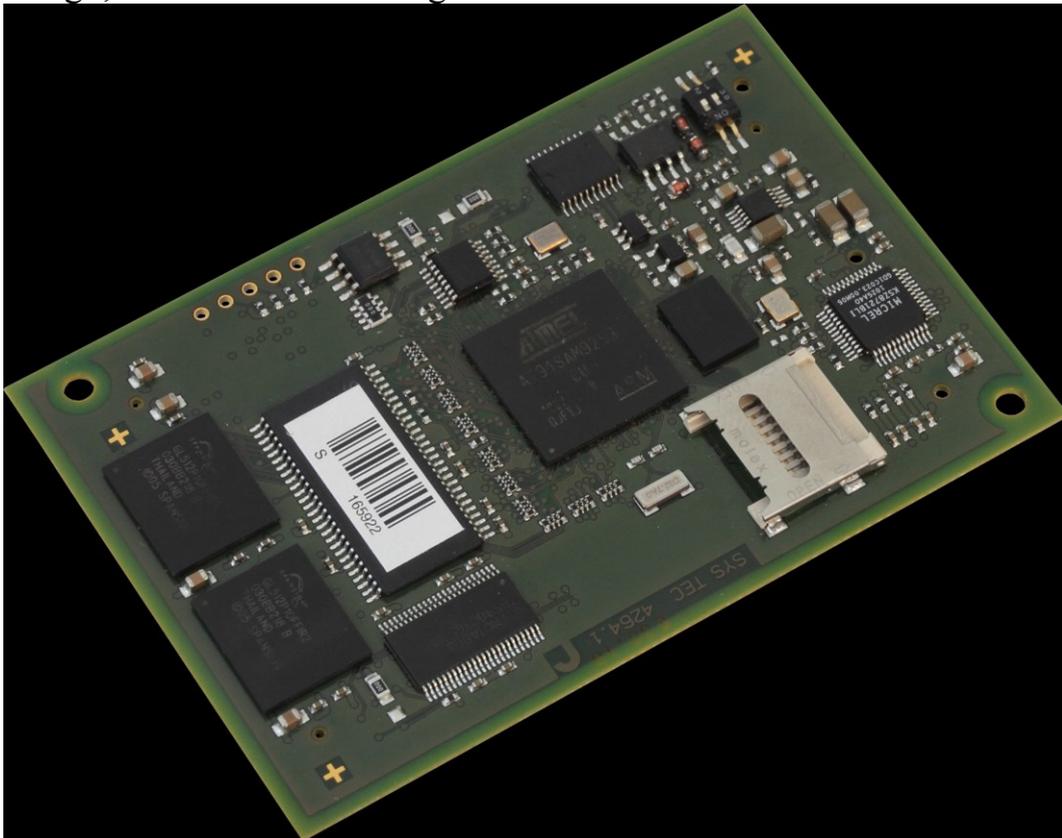


Figure 1: ECUcore-9263

The dimensions of the board are 80mm x 54mm and it includes two board connectors which makes it multifunctional in embedded systems.

The ECUcore-9263 features an Atmel AT91SAM9263 microcontroller. It is a highly-integrated 32-bit microprocessor based on the ARM926EJ-S architecture.

The interconnection to a baseboard is possible through a pair of low-density (2mm pitch) connectors with 200 pins in total.

The ECUcore-9263 includes the following features:

- Internal features of the Atmel AT91SAM9263:
 - Internal 240MHz CPU-clock from external 3-20MHz
 - 16kiB Data- / 16kiB instruction cache, MMU
 - 128k ROM, 96k RAM internal with single cycle access
 - External bus interface for SDRAM, Static memory, NAND- and Compact Flash
 - USB2.0 full speed 1x device, 2x host
 - 1 Fast Ethernet controller MAC
 - Nine 32-bit-layer bus matrix
 - Twenty Peripheral DMA controller channels
 - System controller including Reset controller, Shutdown controller, twenty 32-bit Battery backup registers, Clock generator, Power management controller, Advanced interrupt controller, Debug Unit, Periodic interval timer, Watchdog and Double Realtime timer
 - LCD controller that supports active or passive displays, Resolution up to 2048x2048, Supports virtual screen buffers
 - 2D graphics accelerator, Line draw, Block transfer, Clipping, Commands queuing
 - 1x AC97 controller
 - 3x USART
 - 1x Part 2.0A and Part 2.0B compliant CAN controller
 - 2 Master/Slave SPI with 4 chip selects
 - 1 I2C interface up to 400kbits
 - 1x 3channel 16bit Timer/Counter
 - Multimedia card interface, SD- card and MultiMediaCard™ compliant
 - EmbeddedICE interface
 - 324-ball TFBGA package

- Memory configuration:
 - up to 128MiB 16bit NOR-Flash (default 64MiB)
 - up to 256MiB 16bit NAND-Flash (optional)
 - up to 64MiB 32bit SDRAM (default 32MiB)
 - up to 2MiB 16bit Video RAM (only 1MiB useable)

- Communication features:
 - 1 Ethernet interface
 - 3 UARTs as LVTTL
 - 1 CAN as LVTTL
 - 1 USB device full speed
 - 2 USB host full speed
 - 2 SPI with 4 chip select
 - I²C interface

- Other board-level features:
 - Ethernet PHY
 - Micro SD-Card slot
 - LVDS controller (optional)
 - Touch controller
 - Power failure recognition
 - Battery-buffered Real time clock
 - Temperature sensor
 - SPI EEPROM for data storage 32KiB
 - JTAG/Embedded ICE interface
 - 16MHz main crystal, 32,768kHz low speed crystal
 - 3.3V operating voltage
onboard generated voltage for CPU
 - Industrial temperature range (-40°C to +85°C)
 - RoHS compliant

3.2 Block Diagram

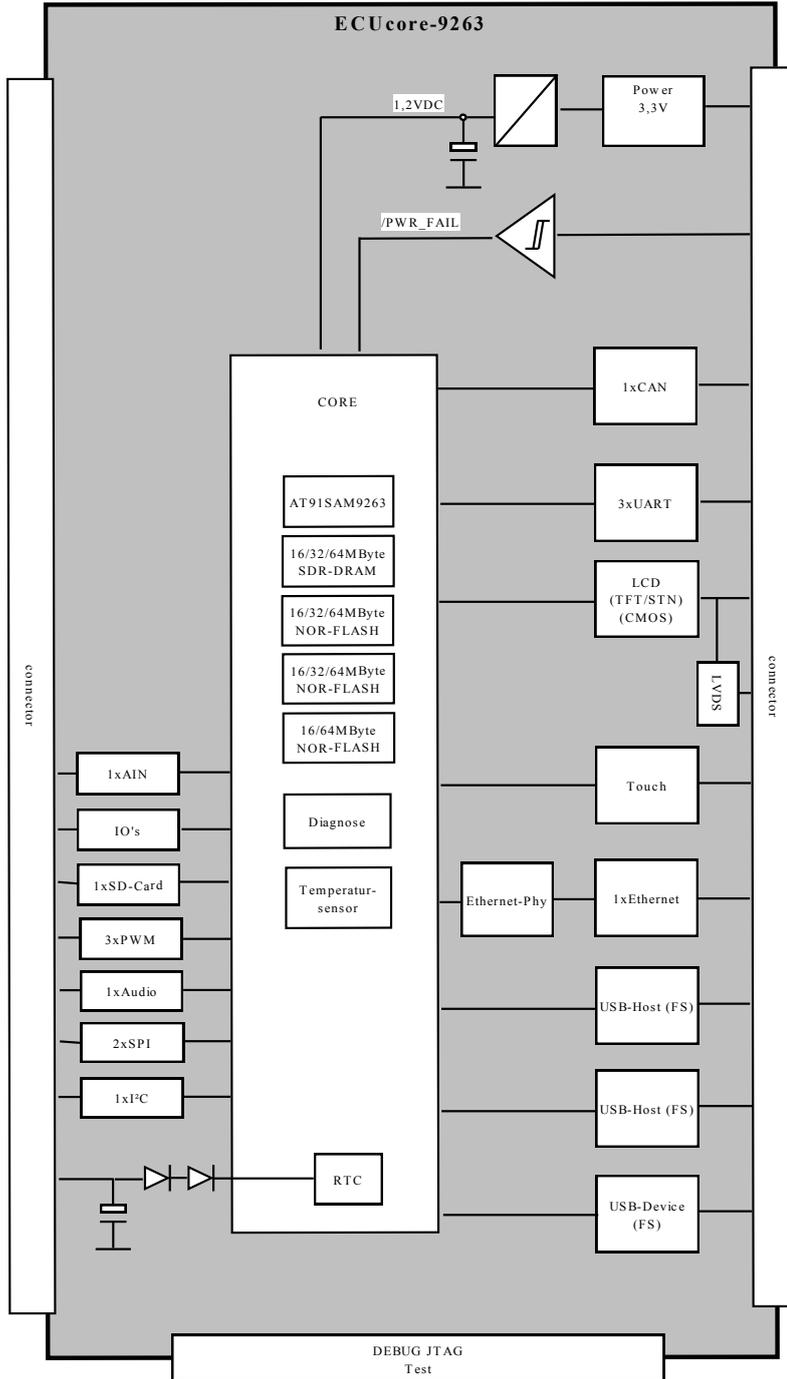


Figure 2: Block Diagram ECUcore-9263

4 Component Descriptions

The functions of the on-board components are explained in the following sections.

4.1 Connectors

The ECUcore-9263 has two board connectors. Each of the SMT socket strips consists of 100 contacts divided into double rows. In total the module has 200 contacts. For better emc-properties, 20% of the pins are GND.

A third connector at the front side is for connecting debug interfaces of the CPU and the signal /DIS_NAND.

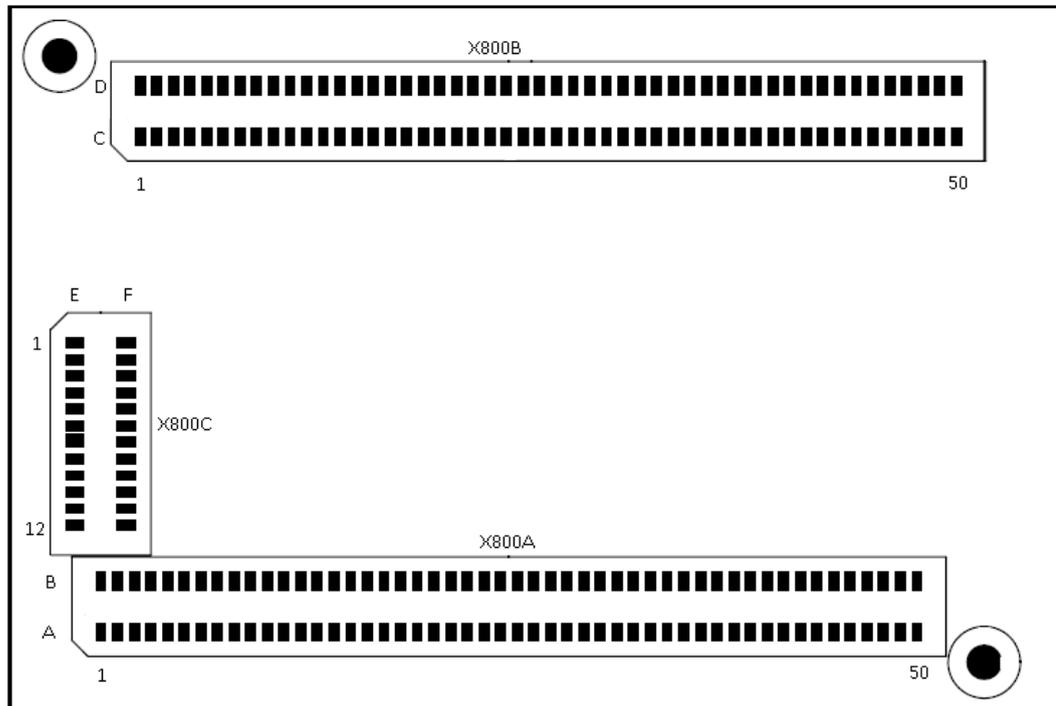


Figure 3: Pinout (top view)

The picture shows the module from top view which means you look from the top through the module. The connectors are placed accordingly to the ones on the baseboard.

The board connectors are equipped with the common and durable 1,27mm pitch. The type of socket stripes used on the ECUcore-9263 is '6060'-series provided by "W+P PRODUCTS" with a height of 3,6mm.

The series matches (e.g.) with "W+P PRODUCTS" strip line series '7072' or '7073'. Please refer to the datasheet and their electrical specifications.

Connectors:

Module: W+P 6060-100-36-00-00-00-PPST (2x50pol. socked))

W+P 6060-024-36-00-00-00-PPST (2x12pol.)

Baseboard: W+P 7072-100-10-00-10-PPST (2x50pol. header)

W+P 7072-024-10-00-10-PPST (2x12pol.)

The following table defines the pinout.

Signal	Pin	Pin	Signal	Signal	Pin	Pin	Signal
GND	A01	B01	GND	GND	C01	D01	+2V5_EPHY
/BOOT	A02	B02	/MR	ETH_TX-	C02	D02	GND
WKUP	A03	B03	/RESET	ETH_TX+	C03	D03	ETH_SPEED
SHDN	A04	B04	/PFI	ETH_RX+	C04	D04	ETH_LINK/ACT
BMS/AC97RX	A05	B05	WDI	ETH_RX-	C05	D05	GND
GND	A06	B06	PCK0	GND	C06	D06	IO_PE10
DRXD	A07	B07	GND	IO_PD11	C07	D07	IO_PE12
DTXD	A08	B08	RTS0	IO_PD15	C08	D08	IO_PE20
RTS2	A09	B09	CTS0	GND	C09	D09	GND
CTS2	A10	B10	RTS1	MCH_DA0	C10	D10	IO_PA22
IO_PE13	A11	B11	CTS1	MCH_DA1	C11	D11	MCH_DB1
GND	A12	B12	GND	MCH_DA2	C12	D12	MCH_DB2
TXD0	A13	B13	TXD1	MCH_DA3	C13	D13	MCH_DB3
RXD0	A14	B14	RXD1	MCH_CK	C14	D14	MCII_CDA
TXD2	A15	B15	IO_PE15	GND	C15	D15	MCII_CDB
RXD2	A16	B16	IO_PE17	SCK0	C16	D16	GND
GND	A17	B17	PCK3	SCK1	C17	D17	TIOA1
USB_HDPA	A18	B18	UDP_VBUS	SCK2	C18	D18	TIOB1
USB_HDMA	A19	B19	GND	PCK1	C19	D19	TIO_PB30
USB_HDPB	A20	B20	USB_DDP	IO_PB31	C20	D20	PWM0
USB_HDMB	A21	B21	USB_DDM	PWM1	C21	D21	TIOB0
GND	A22	B22	GND	PWM2	C22	D22	TCLK0
I2C_DATA	A23	B23	CANTX	BACKL 5/12V	C23	D23	GND
I2C_CLK	A24	B24	CANRX	GND	C24	D24	BACKL_EN
GND	A25	B25	IO_PE16	EXT_TEMP_IN	C25	D25	LCD_SEL_3/5V
/SPI1_CS0	A26	B26	GND	PWM3_BACKL	C26	D26	DISP_ON
/SPI1_CS2	A27	B27	/SPI1_CS1	X_LEFT	C27	D27	Y_LOW
SPI1_MOSI	A28	B28	SPI1_MISO	X_RIGHT	C28	D28	GND

Signal	Pin	Pin	Signal	Signal	Pin	Pin	Signal
/SPI1_CS3	A29	B29	SPI1_SPCK	GND	C29	D29	Y_UP
AC97CK	A30	B30	AC97FS	IN_3	C30	D30	ANALOG_IN
GND	A31	B31	AC97TX	LCD_TXout0+	C31	D31	LCD_TXout0-
/SPI0_CS0	A32	B32	GND	LCD_TXout1+	C32	D32	LCD_TXout1-
/SPI0_CS2	A33	B33	/SPI0_CS1	LCD_TXout2+	C33	D33	GND
SPI0_MOSI	A34	B34	SPI0_MISO	LCD_TXout2-	C34	D34	LCD_TXoutCLK+
/SPI0_CS3	A35	B35	SPI0_SPCK	GND	C35	D35	LCD_TXoutCLK-
IO_PE14	A36	B36	SD_SLOT	LCDD2_R0	C36	D36	LCDD3_R1
GND	A37	B37	MCI0_CK	LCDD4_R2	C37	D37	LCDD5_R3
MCI0_CDB	A38	B38	GND	LCDD6_R4	C38	D38	LCDD7_R5
MCI0_DB0	A39	B39	MCI0_DB1	LCDD10_G0	C39	D39	GND
MCI0_DB2	A40	B40	MCI0_DB3	LCDD11_G1	C40	D40	LCDD12_G2
MATRIX_IO1	A41	B41	MATRIX_IO0	GND	C41	D41	LCDD13_G3
MATRIX_IO3	A42	B42	MATRIX_IO2	LCDD14_G4	C42	D42	LCDD15_G5
GND	A43	B43	MATRIX_IO4	LCDD18_B0	C43	D43	LCDD19_B1
MATRIX_IO5	A44	B44	GND	LCDD20_B2	C44	D44	LCDD21_B3
MATRIX_IO7	A45	B45	MATRIX_IO6	LCDD22_B4	C45	D45	GND
IO_PB22	A46	B46	IO_PB23	LCDD23_B5	C46	D46	/LVDS_PWD
IO_PB24	A47	B47	IO_PB25	GND	C47	D47	LCDDC
VBAT	A48	B48	IO_PB26	LCDDEN	C48	D48	LCDDOTCLK
GND	A49	B49	GND	LCDHSYNC	C49	D49	LCDVSYNC
+3V3	A50	B50	+3V3	/TOUCH_INT	C50	D50	GND

Table 1: Pinout connector X800A/X800B

Pin function:

Name	Function
/BOOT	for selecting software-boot-sequence going till uboot or linux image
/MR	manual reset input of module
/RESET	reset output signal of reset-ic and CPU
/PFI	Power fail input for watching external power supply
WDI	watchdog input
WKUP	wakeup-pin for leaving shutdown mode
SHDN	shutdown-output for signaling shutdown mode
BMS	boot mode select of CPU boot from NOR-Flash or SD-Card, ..., USB
DRXD, DTXD	Debug UART (LV-TTL-level)
TXDx, RXDx, RTSx, CTSx, SCKx	USART 0,1,2 with handshake signals and clock signal (LV-TTL-level)
USB_HDxx	2 channel USB-Host
USB_DDP, USB_DDM	USB-Device
I2C_DATA, I2C_CLK	two wire interface
CANTX, CANRX	CAN (LV-TTL-Level)
VBAT	backup battery input (3,3V) for RTC
ETH0_TX-, TX+, RX-, RX+; +2V5_EPHY	Ethernet-interface with reference voltage
IO_Pxxx	general purpose input / output pin
MCIx_CK, MCIx_CDA, MCIx_CDB, MCIx_DBx	MM-Card interface pin
PWMx	Pulse width modulation output channel
TIOxx	Timer Input/Output
+3V3	3,3V-supply (about 400mA)
GND	Signal ground

Table 2: Signal description connector X800A/X800B

Connector X800C:

Signal	Pin	Pin	Signal
+3V3	1	2	/RESET
/JTAGSEL	3	4	GND
ARM_TDI	5	6	ARM_TDO
ARM_TCK	7	8	ARM_TMS
GND	9	10	ARM_/NRST
ARM_RTCK	11	12	DRXD
DTXD	13	14	GND
/DIS_NAND	15	16	
	17	18	
GND	19	20	
	21	22	
	23	24	GND

Table 3: Pinout connector X800

Pin function:

All JTAG pins for debugging and programming the CPU. The signal /DIS_NAND for disabling boot from NAND flash.

4.2 Switch Configuration

The following figure shows the position of switch S1 which is placed on the top-side of the module.

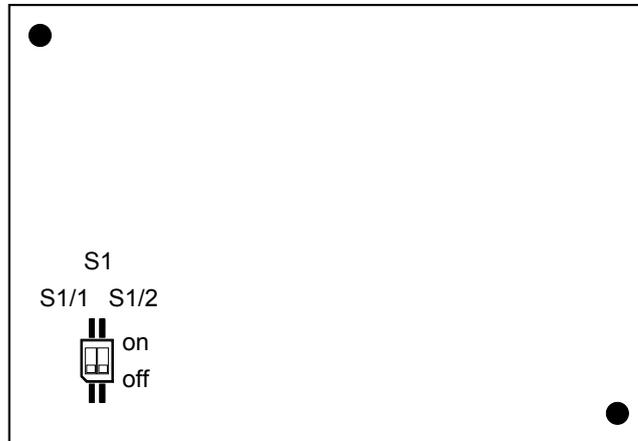


Figure 4: Switch position PCB 4264.2 (PLD)

The function of S1 depends on the application. Please refer to the software manual for further information.

The following table lists the switch and its function on the ECUcore-9263.

Switch	Setting	Signal	Function
S1/1	on	/BOOT	application defined default: software starts only till bootloader uboot; the NAND flash is deactivated
	off		software starts till linux; the NAND flash is active
S1/2	on	/BMS	cpu starts from external NOR flash (uboot, Linux)
	off		cpu starts from internal rom (atmel bootloader) or NAND flash, if it is active

Table 4: Overview of the Switch

4.3 Power Supply

The ECUcore-9263 must be supplied with an input voltage of +3.3VDC. The typical current consumption is approximately 400mA.

The 3,3V directly supplies:

- AT91SAM9263 IO voltage
- Flash, RAM, EEPROM
- RTC, Temperature sensor
- Micro SD card
- Ethernet PHY
- Touch controller, LVDS controller

So be careful and provide a good voltage with low tolerance and low ripple. See "Technical Data" for detailed information.

The onboard switching regulator generates all other needed voltages which is:

- 1,2V for SAM9263 core voltage

4.4 Reset Controller

Functions of the Reset Controller:

- watching 3,3V system voltage and reset the module if the voltage is too low
- monitoring power fail input from baseboard
- manual reset input and stretched reset output
- 1,0sec watchdog timer

Watching voltage

Voltage	Min Level
3,3V	3,1V

a) Watchdog

The Trigger-Pin 'WDI' is connected to the socket stripe X800A/B5. Any ECUCore pin can be connected externally to WDI. Leaving WDI floating disables the watchdog.

b) Power fail

The power fail input of the Reset controller is connected to the socket stripe pin X800A/B04 with 1M pullup to 3,3V. If the voltage at /PFI falls below 1,25V, the /PFI_INT switches to low.

An external digital signal can be used to trigger a power fail interrupt. This can be the power good output (e.g. open collector output) of a power supply.

c) Manual Reset

The manual reset (/MR) is connected to X800A/B02 with 10k pullup to 3,3V. A reset occurs if the manual reset is switched to GND.

If a reset occurs, /RESET remains low for 200ms. The reset out pin is connected to X800A/B03.

4.5 Chip Configuration after Reset

The start vector depends on the switch S1/2. If the switch is on (default), the CPU starts from the external Flash with the uboot-bootloader.

AT91SAM9263 starts with a startup configuration with fixed buswidth, busfrequency, timing and control signals. Changes are not possible via configuration pins.

If the switch S1/2 is off, the CPU starts from the internal ROM with the Atmel-bootloader. Afterwards, peripheral devices (serial Flash, SDcard, NAND flash) are checked for executable code. If no valid application is found, SAM-BA Boot is executed afterwards. It waits for transactions either on the USB device, or on the DBGU serial port.

You can only boot from NAND flash whether the switch S1/1 is off, because only so the NAND flash is active!

Both, main and slow clock crystals are mounted. So a precise slow clock is available, needed for download via USB with SAM-BA. The slow clock mode is also possible for power saving applications.

4.6 SDRAM

The AT91SAM9263 has two external bus interfaces up to 32bit demultiplexed. The first interface is shared by SDRAM and Flash.

Two 16bit-Synchronous DRAMs are mounted and connected as one RAM with 32bit-buswidth.

The RAM density by default is 2x16MiB, but layout provides RAM densities up to 2x32MiB.

By default, a RAM with 7,5ns cycle time for 133MHz busfrequency is mounted. It supports the PC133 bus mode of CPU.

4.7 NOR-Flash

The board is equipped with NOR-Flash because it provides a higher security in terms of data retention compared to NAND-Flash. NAND-Flash works with bad sectors can be problematic if such sector influences the boot-up routine of the module in early time. The module is designed for industrial applications with high requirements for safe operation.

The Flash (default: 1x Spansion S29GL512P) is connected via a 16bit bus. It works with 25ns access time. The density by default is 64MiB. It is possible to use up to 128MiB (by mounting a second Spansion S29GL512P on the board); it is limited by the address range of the CPU.

4.8 NAND-Flash

As an option it is possible to mount up 256 MiB of NAND-Flash (default 1x MT29F2G16ABAEAWB) on the board. It can be used as mass storage area and is connected via a 16bit bus to the AT91SAM9263.

4.9 Ethernet Controller

The AT91SAM9263 supports one 10/100 Ethernet channel by an internal MAC with MII/RMII interface.

An onboard PHY chip KSZ8721BLI from Micrel allows for a 10/100 physical interface. The PHY is connected with the RMII interface of the CPU.

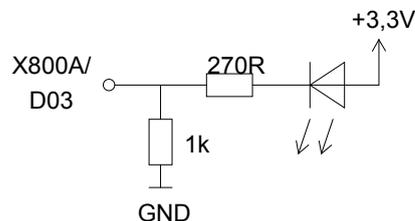
Board connector signals are:

Signal	Description
ETH_TX+	Tx+ from PHY
ETH_TX-	Tx- from PHY
ETH_RX+	Rx+ from PHY
ETH_RX-	Rx- from PHY
2V5_EPHY	2,5V PHY-Supply as reference for transformer
ETH_LINK/ACT	output of PHY-LED0 lowactiv
ETH_SPEED	output of PHY-LED1 lowactiv

Table 5: Ethernet signals

Connect ETH_LINK/ACT and ETH_SPEED LED with a 270R series resistor, not directly!

The ETH_SPEED LED is also a strapping pin, which means that this pin is read at reset. When the pin is open (or high with LED), the PHY is configured for 100MBbps Speed. If you need 10MBbps, place a 1k pulldown resistor to GND at this pin.



Tx and Rx Signals are pulled up with 49,9R to 2,5V-EPHY onboard. So you need only the transformer and connector as external components for communication.

SYS TEC electronic has acquired a pool of these MAC addresses. The MAC address for the first Ethernet interface Eth0 is barcode-labelled and attached on the ECUcore-9263.

4.10 I2C Module

The ECUcore-9263 features one I2C interface. This is a 2-wire serial bus used for communication with I2C devices. The bus is brought out via the board connector. The ECUcore-9263 comes with two onboard I2C devices. Please refer to the table below.

I2C device	Address
Real-Time-Clock Epson 8564JE (U201)	0xA2
Temperature Sensor TI TMP101 (U202)	0x90 (default) 0x91 upon request 0x92 upon request

Table 6: I2C Components

The I2C module defaults to GPIO after reset. The GPIO module has to be configured to enable the peripheral function of the appropriate pins prior to configuring the I2C-Module.

4.10.1 Real Time Clock

The ECUcore-9263 is equipped with a Real time clock to manage real-time applications. The device offers functions such as calendar clock, alarm and timer. It also outputs pre-defined frequencies (32.768kHz, 1024Hz, 32Hz, 1Hz) via the CLKOUT pin.

RTC characteristics:

- Built-in crystal running at 32768Hz
- Programmable alarm, timer and interrupt functions
- Low power consumption:

- Bus active: $\leq 1\text{mA}$
- Bus inactive, CLKOUT inactive: $\leq 1\mu\text{A}$

The Real time clock is supplied with 3.3V DC. If the system voltage is off, a backup battery or cap (connected at X800/A48) supplies the RTC. This battery or cap must be placed on the baseboard.

Device address:

- 0xA2 when write mode
- 0xA3 when read mode

The pin CLKOE is connected to 3.3V DC. So the clock output can be enabled by setting the bit 'FE' in register 'Clock Out frequency' to 1.

CLKOUT and RTC_INT are connected to AT91SAM9263 to be used by the application.

Signal	Pin at AT91SAM9263
CLKOUT	Pin M1 (PE18)
/RTC_INT	Pin G14 (PB20)

4.10.2 Temperature Sensor

The ECUcore-9263 features an optional Temperature sensor TMP101 to record ambient temperatures to, e.g, enable protection from overheating. The ECUcore-9263 just provides the physical connection between the CPU and the sensor. The communication or any protective measures are software functions to be provided by the user application.

The address is adjustable by a resistor. The following table shows the various assembly options.

Resistor	ADD0 signal	Address
R208 equipped (default)	0 (GND)	1001000x = 0x90
R208 open	floated	1001001x = 0x91
R209 equipped (upon request)	3,3V (3V3)	1001010x = 0x92

Table 7: Temperature Sensor Address

Temperature sensor characteristics:

- Temperature resolution of 0.0625°C
- Temperature range of -55°C to +125°C
- Alert pin as interrupt source if temperature exceeds defined limits

The Alert-Pin is connected to AT91SAM9263 to be used by the application (Pin H12 (PB19)).

4.11 SPI Module

The ECUcore-9263 allows high-speed serial communication with SPI devices such as EEPROM via two SPI interfaces. The SPI interfaces contain four chip select (CS) signals each. The SPI bus signals are directly dumped via the board connector.

There is an EEPROM connected to the SPI onboard. The onboard EEPROM is connected to SPI0 and occupies CS0. Furthermore, the onboard touch controller is connected via the SPI0. The touch controller occupies CS3.

The following table shows the available SPI signals.

X800-Pin	Connector signal	SPI signal	Description
A32, B33, A33 A35	/SPI0_CS0 /SPI0_CS1 /SPI0_CS2 /SPI0_CS3	/SPI0_CS0 /SPI0_CS1 /SPI0_CS2 /SPI0_CS3	SPI-ChipSelect (CS3, CS0 used onboard)
A34	SPI0_MOSI	SPI_MTSR (SOUT)	Master Transmit Slave Receive
B34	SPI0_MISO	SPI_MRST (SIN)	Master Receive Slave Transmit
B35	SPI0_SPCK	SPI_CLK (SCK)	Clock
A26 B27 A27 A29	/SPI1_CS0 /SPI1_CS1 /SPI1_CS2 /SPI1_CS3		SPI-ChipSelect
A28	SPI1_MOSI	SPI_MTSR (SOUT)	Master Transmit Slave Receive
B28	SPI1_MISO	SPI_MRST (SIN)	Master Receive Slave Transmit
B29	SPI1_SPCK	SPI_CLK (SCK)	Clock

Table 8: SPI Signals

4.11.1 Onboard EEPROM

The ECUcore-9263 is equipped with an onboard EEPROM. The EEPROM (default AT25256AN 32KiB) can be used to store user data. It is connected to the AT91SAM9263 via SPI module SPI0. The EEPROM uses chip select CS0 of SPI0.

The EEPROM supports SPI Modes 1 and 3. There is no separate erase cycle needed before writing.

4.11.2 Touch Controller

To support Touch screen application the ECUcore 9263 features an on board touch screen interface. This interface is realized by the ADS7846E from Texas Instruments. The touch controller is connected to the SAM9263 via the SPI module SPI0. It uses the chip select CS3 of SPI0.

The following table shows the available signals of the touch controller on connector X800.

X800-Pin	Connector signal	Touch controller signal	Description
C27	X_LEFT	X+	X+ Position input
C28	X_RIGHT	X-	X- Position input
D29	Y_UP	Y+	Y+ Position input
D27	Y_LOW	Y-	Y- Position input
C50	/TOUCH_INT	/PENIRQ	Pen interrupt
C30	IN_3	IN3	Auxiliary input 1
D30	ANALOG_IN	IN4	Auxiliary input 2

Table 9: Touch controller signals

The BUSY signal of the ADS7846 is connected to the SAM9263 via pin T6 (PA31) onboard directly. Additionally the /PENIRQ signal of the ADS7846 is directly connected to pin K16 (PA15) of the SAM9263 onboard.

4.12 Display Support

To simplify the development of devices that require human machine interfaces, the ECUcore-9263 supports interfacing LCD and TFT displays directly. The ECUcore-9263 always includes an LCD controller and additional video ram for usage as display frame buffer.

Optionally the ECUcore-9263 can be equipped with an LVDS controller to support longer distances between the ECUcore-9263 board and the connected display.

4.12.1 Video RAM

The Video RAM of the ECUcore-9263 is connected via the second external bus interface using a 16bit wide bus of the AT91SAM9263.

The Video RAM (default: 1x MT45W1MW16PDGA) provides 2MiB of frame buffer memory.

4.12.2 LCD Controller

The AT91SAM9263 features an onchip LCD controller. It consists the logic of transferring LCD image data from an external display buffer to an LCD module with integrated common and segment drives.

The LCD controller supports single and double scan monochrome and color passive STN LCD modules. It also supports single scan active TFT LCD modules. Resolutions up to 2048x2048 pixels can be driven. The maximum pixel depth without any restrictions is 18bits (6bits per pixel). Higher pixel depths are only possible if the onboard Ethernet controller is disabled.

The ECUcore-9263 is designed to use a maximum pixel depth of 18bits. The following table shows the signals that are dumped out of the board via X800

X800-Pin	Connector signal	Description
C36, D36, C37, D37, C38, D38	LCDDx_Rx	LCD data bus output (red)
C36, C40, D40, D41, C42, D42	LCDDx_Gx	LCD data bus output (green)
C43, D43, C44, D44, C45, C46	LCDDx_Bx	LCD data bus output (blue)
D47	LCDDC	Contrast control signal
C48	LCDDEN	Data enable signal
D48	LCDDOTCLK	LCD clock signal (STN/TFT)
C49	LCDHSYNC	Line synchronous signal (STN) or Horizontal synchronous signal (TFT)
D49	LCDVSYNC	Frame synchronous signal (STN) or Vertical synchronization signal (TFT)

Table 10: LCD controller signals

The pins can be connected directly to an appropriate passive STN LCD or active TFT LCD module.

4.12.3 LVDS Controller

Upon request the ECUcore-9263 can be equipped with an LVDS controller (DS90C365AMT from National). The LVDS controller is useful, if the display has to be connected by longer wires to the ECUcore-9263 or if there are higher requirements for disturbance resistance. The following table shows the available signals of the LVDS controller.

X800-Pin	Connector signal	LVDS controller signal
C31	LCD_TXout0+	TXOUT0+
D31	LCD_TXout0-	TXOUT0-
C32	LCD_TXout1+	TXOUT1+
D32	LCD_TXout1-	TXOUT1-

C33	LCD_TXout2+	TXOUT2+
C34	LCD_TXout2-	TXOUT2-
D34	LCD_TXoutCLK+	TxCLK OUT+
D35	LCD_TXoutCLK-	TxCLK OUT-
D46	/LVDS_PWD	PWDN

Table 11: LVDS controller signals

The power down signal /LVDS_PWD of the LVDS controller is pulled up by 10k onboard. To enter power down mode of the LVDS controller the /LVDS_PWD signal can be pulled low by externally connecting any general purpose output pin to that signal.

4.13 Audio Controller (AC97)

There is one AC97 Audio controller on the ECUcore-9263. It is provided by the AT91SAM9263 on chip peripherals. The Audio controller is compliant with AC97 Component Specification 2.2.

The AC97 Controller features a peripheral DMA controller for audio streaming transfers and supports variable sampling rate and four PCM sample resolutions. All pins of the AC97 mode are dumped of the board via X800 as LVTTL level. Please refer to the following Table

X800-Pin	Connector signal	AC97 signal	Description
A05	BMS/AC97RX	AC97RX	Receiver data
B31	AC97TX	AC97TX	Transmitter data
B30	AC97FS	AC97FS	48 KHz frame indicator and synchronizer
A30	AC97CK	AC97CK	12,288 Mhz bit-rate clock

Table 12: AC97 Signals

Externally the AC97 codec can be connected directly to these signals. The AC97RX signal is shared with the BSM signal.

That means the level of the AC97RX signal is evaluated at boot time by the AT91SAM9263 to select boot mode. Depending on S1/2 this signal is either pulled up with a 100k resistor or pulled down with a 1k resistor.

After booting, the AC97RX can be used for receiving AC97 data by the application.

4.14 CAN Interface

The ECUcore-9263 includes one CAN interface. It is realized by the onchip CAN controller of the AT91SAM9263. The CAN bus is brought out via the board connector as LVTTL interface.

Externally a 3,3V CAN transceiver can be directly connected to CAN. Alternatively, a galvanic decoupled CAN interface can be built to save the module for EMC.

4.15 Serial Interface

The AT91SAM9263 supports up to 3 independent USARTs. They feature individual baudrate generators, IrDA[®] infrared modulation / demodulation, Manchester encoding / decoding, support for ISO7816 T0/T1 Smart card, hardware handshaking and RS485 support

All USARTs are available on the board connector with the following lines: RXD, TXD, CTS, RTS and SCK.

All signals are brought out with LVTTL-Level. They are used to interface serial communication via RS232, RS422 or RS485 by external transceivers.

4.16 SDCard/MMC Interface

The AT91SAM9263 has two two-slot multimedia-card interfaces which means the two interfaces use one clock. Slot B of the first MMC interface (MCI0) and slots A and B of the second MMC interface (MCI1) are brought out via connector. Each interface has 4 data pins for the usage as SDCard or MMC interface. The onboard SD card connector is connected to slot A of MCI1.

Card Detect and Card Protect are not supported by default. Use general purpose IO Pins to watch these signals.

MicroSD sockets only provide SLOT-contact to indicate a closed socket. This signal of the onboard SD Card slot is connected to PB6 of the SAM9263. It is also available at pin X800A/B32. The SLOT-contact can be watched by the software.

If the SLOT contact is used, the MMC interface MCI0 slot A can not be used to interface a SD/MMC card. If the NAND-Flash option of the board is present, the slot B of MCI1 can not be used because the MCI1_DB0 (IO_PA22) is occupied by the NAND-Flash.

4.17 USB Interfaces

The AT91SAM9263 provides one USB2.0 (12Mbit/s) device and two USB2.0 (12Mbit/s) host interfaces. Each interface is brought out at the connector with its P and M signal.

No security components (such as TVS-Diodes) are provided at the module, they have to be mounted near the USB connector on the baseboard.

Overcurrent protection is not supported by default. If necessary, use an external current limiting IC with overcurrent-flag and connect it to one of the AT91SAM9263 general purpose IOs.

4.18 Embedded ICE Port

The Embedded ICE-Port is not provided by the series module. It requires the socket stripe X800C. This connector is not mounted.

ECUcore-9263 is supposed for programming in Linux. There is no hardware debugging needed at all. For a Debug at this interface, a separate Debugger is needed as well.

Through the mounting process and while using the connector, the ARM_x signals are relevant for ICE and have to be connected to the debugger. No pullups or pulldowns are required. Pullups 4k7 are mounted onboard at /NRST, TDI, TMS and TCK.

The /JTAGSEL pin is for selecting the ICE or JTAG mode. The JTAG mode is for the usage with BoundaryScan hardware and not needed for debugging. So leave open the pin when using ICE! For using JTAG, put it to GND.

5 Technical Data

The physical dimensions of the ECUcore-9263 is shown in the figure below.

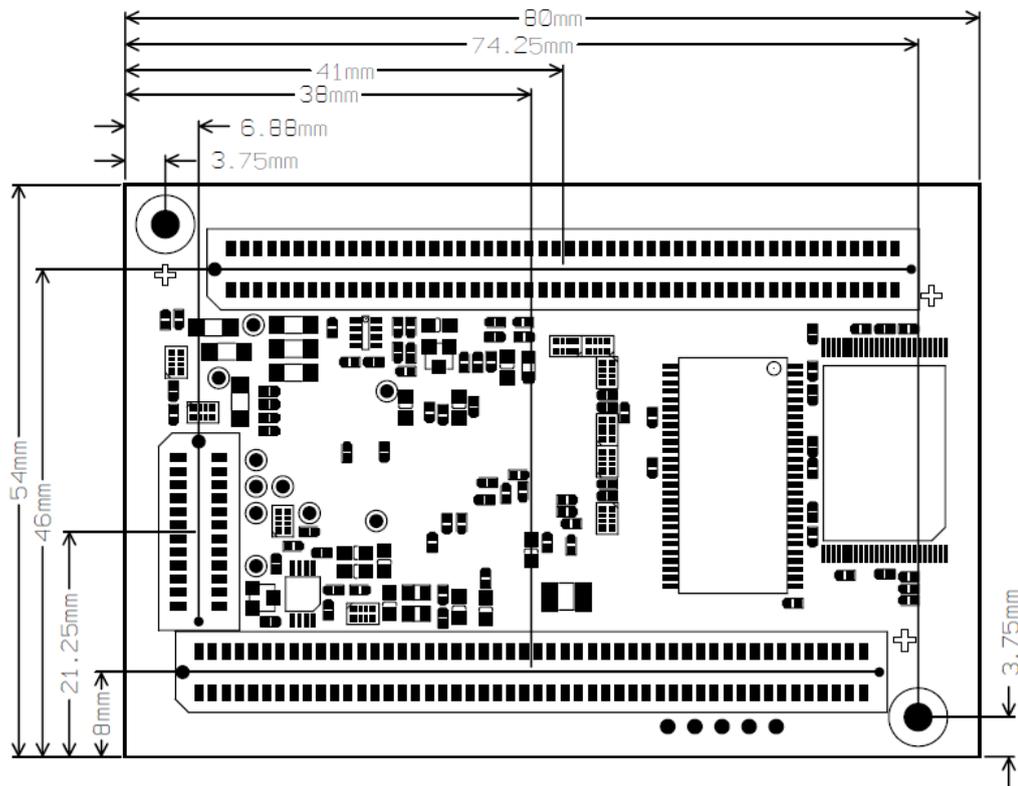


Figure 5: Physical Dimensions

The height including the board connector and components is about 9mm. The thickness of the PCB is about 1.6mm. The maximum component height on top is about 3mm.

dimensions	80mm x 54mm x 8mm
weight	approximately 21,5g
operating temperature	-40°C to +85°C
storage temperature	-40°C to +85°C
operating voltage	3.3V DC \pm 5%
current consumption	typ. 400mA
I/O-Level	3.3V DC \pm 5%

Table 13: Technical Data

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Did you find any mistakes in this manual? _____ page

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Return to: SYS TEC electronic GmbH
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D-07973 Greiz
GERMANY
Fax : +49 (0) 36 61 / 62 79 99

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